IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An integrated circuit, comprising:

a clock driver disposed on the integrated circuit;

a clock grid disposed on the integrated circuit, wherein the clock driver is disposed outside a region of the clock grid; and

at least one interconnect arranged to directly propagate a signal from an output of the clock driver past an exterior region of the clock grid to a connection point residing at a non-exterior region of the clock grid.

2. (Previously Presented) The integrated circuit of claim 1, wherein the connection point is positioned such that a component operatively connected to the clock grid at the connection point receives a signal from the clock driver at the connection point, where the signal at the connection point has less skew than if the connection point was positioned at an edge of the clock grid.

3. (Previously Presented) The integrated circuit of claim 1, wherein the at least one interconnect is arranged in a wire tree configuration.

4. (Previously Presented) The integrated circuit of claim 3, wherein the wire tree configuration is balanced.

5. (Currently Amended) A computer system, comprising:

an integrated circuit having a clock grid;

at least one clock driver that provides a clock signal to the clock grid, wherein the at least one clock driver resides outside a region of the clock grid; and

a transmission structure arranged to ~~carry~~directly propagate the clock signal from an output of the at least one clock driver past an exterior region of the clock grid to at least one point residing at a non-exterior region of the clock grid.

6. (Previously Presented) The computer system of claim 5, wherein the at least one point is positioned such that a component operatively connected to the clock grid at the at least one point receives a signal from the clock driver at the at least one point, where the signal at the at least one point has less skew than if the at least one point was positioned at an exterior region of the clock grid.

7. (Previously Presented) The computer system of claim 5, wherein the transmission structure has a wire tree configuration.

8. (Previously Presented) The computer system of claim 7, wherein the wire tree configuration is balanced.

9. (Currently Amended) A method for reducing clock skew, comprising:

sending a clock signal from a clock driver to a first component through a connection point on a clock grid, wherein the clock driver resides outside a region of the clock grid; and

sending the clock signal from the clock driver to a second component through the connection point,

wherein the clock signal is directly propagated from an output of the clock driver past an exterior region of the clock grid to the connection point, and

wherein the connection point is at a non-exterior region of the clock grid.

10. (Previously Presented) The method of claim 9, wherein the clock signal received by the first component and the second component has less skew than if the connection point was at an edge of the clock grid.

11. (Canceled)

12. (Canceled)

13. (Currently Amended) A transmission structure for driving a signal onto a clock grid, comprising:

an interconnect connecting a clock driver to the clock grid, wherein the clock driver resides outside of a region of the clock grid,

wherein the interconnect directly connects the clock driver past an exterior

region of the clock grid to a connection point residing at a non-exterior region of the clock grid.

14. (Previously Presented) The transmission structure of claim 13, wherein the transmission structure is balanced.

15. (Previously Presented) The transmission structure of claim 13, wherein the interconnect is arranged in a wire tree configuration.